# Reduced Intermodulation Distortion of AlGaAs/InGaAs Doped-Channel FETs by Air-bridge Gate Process

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***Abstract*** Conventional mesa isolation process in AlGaAs/InGaAs doped-channel FETs results in the gate contacting the exposed highly n-type doped channel at the mesa sidewall, forming a parasitic gate leakage path. In this report, we suppress the gate leakage from the mesa-sidewall to increase the gate-to-drain breakdown voltage ($BV_{gd}$) and the microwave power performance by using the air-bridge gate structure. The device gate leakage characteristics under high input power swing are particularly investigated in terms of the 3rd-intermodulation distortion, which are sensitive to the sidewall gate leakage. The air-bridge gate DCFETs provide not only a lower power gain at higher input powers but also a lower IM3 power than those characteristics in conventional DCFETs.

## I. INTRODUCTION

The advance of mobile communication system and the rapid growth of various wireless services, have led to a huge growth of RF power devices. The requirements of modern wireless communication systems place stringent demands on the linearity of power devices. The continuous drive to decrease power consumption in cellular phones has placed the most important issues on the high efficiency power transistors used in wireless communication. Based on our previous investigations, heterostructure doped-channel FETs (DCFETs) have demonstrated better device linearity, higher current density, and higher gate breakdown as well as higher turn-on voltages as compared to HEMTs and MESFETs [1, 2]. However, under a high input RF power swing, the gate leakage will be enhanced due to the presence of the mesa edge contacting problem, which results in an output power compression and a intermodulation distortion [3]. In this study, we have successfully fabricated the air-bridge gate DCFETs (A-DCFETs) by using a second mesa etch method to achieve an excellent Schottky gate performance,which can suppress the gate leakage current under a high input signal swing. The output power compression and 3rd-order intermodulation distortion of A-DCFETs and DCFETs were characterized to investigate the performance influenced by the air-bridge gate approach.

## II. DEVICE STRUCTURES AND FABRICATION

$Al_{0.3}Ga_{0.7}As/In_{0.15}Ga_{0.85}As/GaAs$ DCFETs, shown in Fig. 1, were grown by molecular beam epitaxy (MBE) on (100)-oriented semi-insulating GaAs substrates. Two 15 nm thick pseudomorphic $In_{0.15}Ga_{0.85}As$ doped channels ($n = 2\times10^{18}$ $cm^{-3}$) were grown on top of a 300 nm thick undoped GaAs buffer layer, and a 5 nm undoped GaAs layer was inserted between these two InGaAs channels. Finally, a 20 nm $n^+$-GaAs cap layer was grown to improve the ohmic contact resistivity.

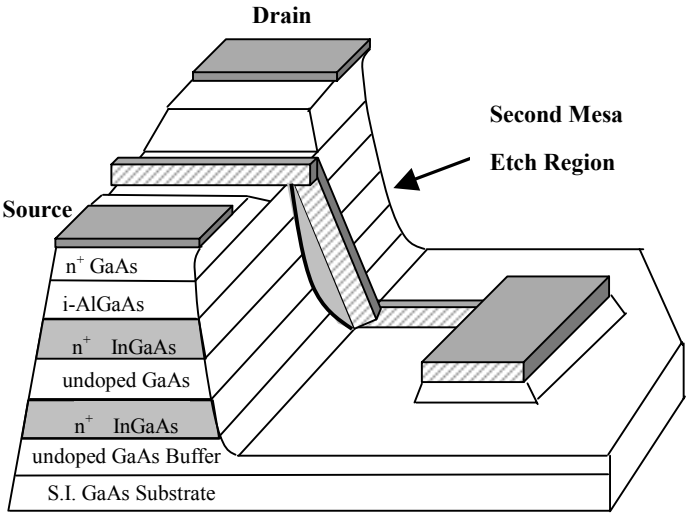


Fig.1 The 3-D perspective of the Air-bridge gate AlGaAs/InGaAs DCFETs

For device fabrication, ohmic contacts of AuGeNi/Ti/Au metals were deposited by e-beam evaporation and patterned by conventional lift-off processing. An $NH_4OH/H_2O_2/H_2O$ solution was used for mesa etching reaching the GaAs buffer layer. As to

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the gate recess process, instead of using traditional wet etching, we applied the optimum reactive ion etching to achieve a high uniformity and yield. After etching away the top $n^+$-GaAs layer and partial undoped AlGaAs layer, 1.0 μm long Ti/Au-gates were deposited by a lift-off process. In order to achieve an air-bridge gate, shown in Fig.1, a second mesa etching was performed in the DCFETs after the gate deposition. The active region of the device was protected by photoresist and $NH_4OH/H_2O_2/H_2O$ (3:1:100) was used for chemical etching.

## III. DEVICE DC AND MICROWAVE POWER PERFORMANCE

Fig. 2 shows the characteristics of the Schottky gate performance of A-DCFETs and DCFETs, respectively. The breakdown voltage (gate reversed current =1mA/mm) of A-DCFETs is increased from 8.2 V to 10.2 V. The gate leakage current for A-DCFETs is significantly reduced by an order of magnitude, owing to the elimination of sidewall gate leakage path directly from gate to channel. Thus, this leakage current in mesa sidewalls results in a soft breakdown mechanism.

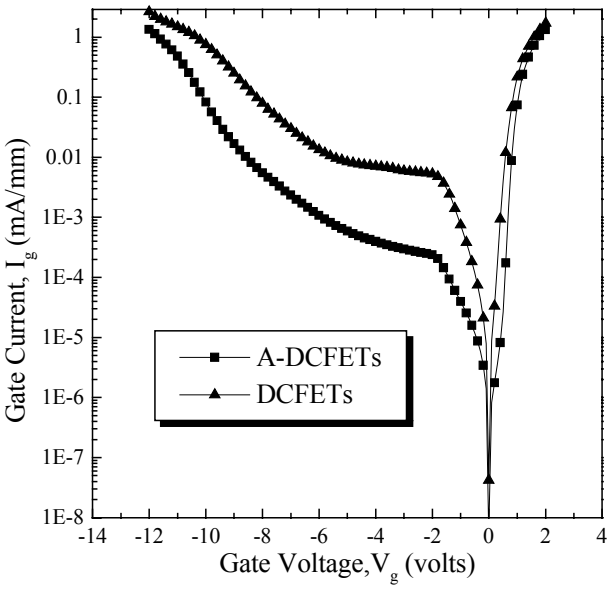



Fig. 2 Schottky diode characteristics of conventional and air-bridge gate DCFETs.

As to the transistor performance, Fig. 3(a) shows the comparison of drain-to-source current ($I_{ds}$) versus drain-to-source voltage ($V_{ds}$) between A-DCFETs and conventional DCFETs with a 1.0 μm-long gate. It is clear that the knee voltages of A-DCFETs are improved, which will be beneficial to device power performance. Fig. 3(b) shows the $V_{gs}$ dependence of transconductance ($g_m$) and $I_{ds}$ curves for A-DCFETs and DCFETs. The maximum $I_{ds}$ and $g_m$ are 835 mA/mm, 240 mS/mm for A-DCFETs, and 750 mA/mm, 226 mS/mm for DCFETs, respectively. A flat and uniform $g_m$ distribution of A-DCFETs, as compared with DCFETs is observed, indicating that the A-DCFETs reveal lower leakage current and demonstrate a better device linearity than those results in DCFETs. Furthermore, the $I_{ds}$ versus $V_{gs}$ voltage profiles show a lower $I_{ds}$ suppression in the forward biased range, and the constant $g_m$ expands into positive bias for A-DCFETs, which are not the cases of DCFETs.

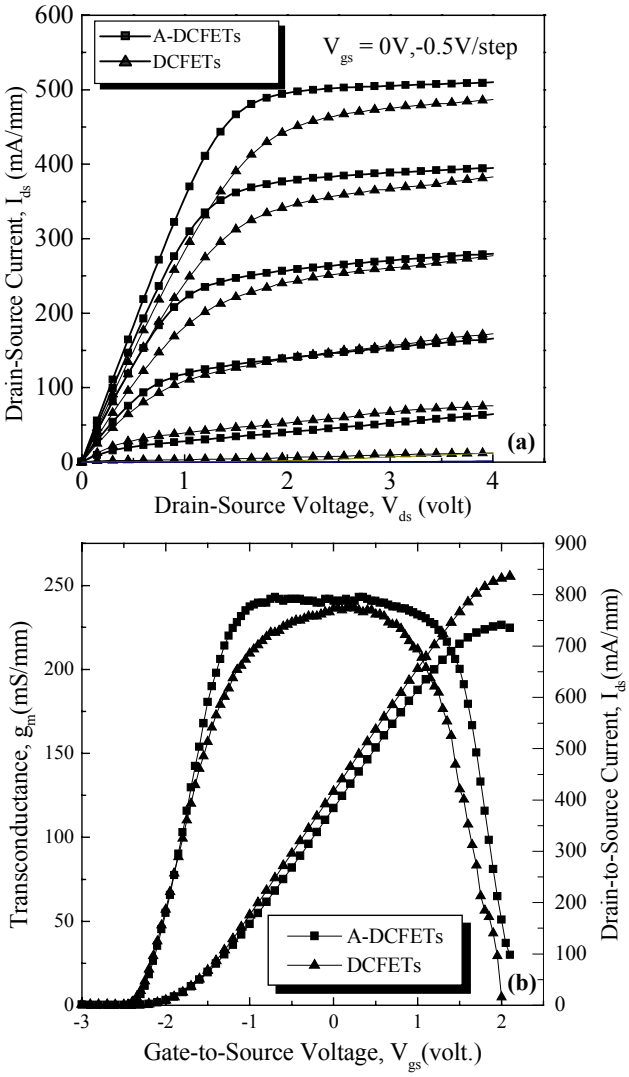



Fig. 3 I-V characteristics (a), $g_m$ and $I_{ds}$ versus $V_{ds}$ characteristics (b) of A-DCFETs and DCFETs for a gate-length of 1.0 μm .

In order to further characterize the devices linearity properties, we used the polynomial curve fitting technique to investigate these transfer characteristics. A 5th order polynomial equation was used to express devices $I_{ds}$-$V_{gs}$ transfer curves, as followings [6]:

$$I_{ds} = a_0 + a_1 V_{gs} + a_2 V_{gs}^2 + a_3 V_{gs}^3 + a_4 V_{gs}^4 + a_5 V_{gs}^5 \quad (1)$$

where $a_0$ means $I_{ds}$ corresponding to $V_{gs}$= 0 V, and $a_1$ represents the linear term of output $I_{ds}$ versus input $V_{gs}$.

For a better linearity of devices, the higher order constants (>$a_1$) should be minimized, and we used these nonlinear constant divided by $a_1$ to represent the index of device linearity, which are shown in Table. 1. The $a_3/a_1$ value, presenting the 3rd-order inter-modulation term, is 0.025 for DCFETs, and is only 0.015 for A-DCFETs. Based on this analysis approach, A-DCFETs demonstrate much better linearity characteristics than conventional DCFETs, indicating that this air-bridge gate technology can assure a lower inter-modulation distortion and suppress signal interference in digital communication systems.

| $a_n$'s | $a_0$ | $a_1$ | $a_2/a_1$ | $a_3/a_1$ | $a_4/a_1$ | $a_5/a_1$ |
|---|---|---|---|---|---|---|
| **A-DCFETs** | **360** | **207** | **-0.014** | **0.015** | **0.0085** | **-0.006** |
| **DCFETs** | **330** | **202** | **0.018** | **0.025** | **0.0095** | **-0.008** |

Table. I Device non-linear terms of I-V transfer curves for both A-DCFETs and DCFETs.

Microwave on-wafer S-parameters for 1.0 μm-long gate devices were measured by an HP-8510 network analyzer. We obtained a maximum $f_T$ ($f_{max}$) of 13 (32) GHz for A-DCFETs and 10.5 (28) GHz for DCFETs at $V_{ds}$=3 V, as shown in Fig.4, respectively. By extracting the small-signal equivalent circuit model, we obtained a $C_{gs}$ of 3.1pF/mm ($C_{gd}$ of 0.15pF/mm) for A-DCFETs and 3.8 pF/mm (0.21 pF/mm) for DCFETs. The reduced parasitic capacitances in A-DCFETs are beneficial to device $f_T$ and $f_{max}$ performance as well as to device linearity. [4].

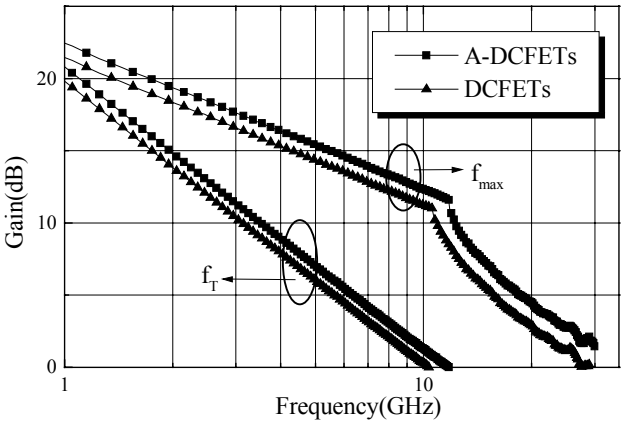



Fig. 4 Current gain and maximum available gain versus frequency for a $1 \times 100 \mu m^2$ device.

The microwave power measurement were performed by a load-pull ATN system with automatic tuners to measure the optimum load impedance for maximum output power. Microwave load-pull power performance was measured at 2.4 GHz with a drain bias of 3.0V for both devices. The device was operated at a class AB (1/8 $I_{dss}$), which is compromised by considering device power-added efficiency (PAE) and output power. Fig.5 shows the gate leakage current versus input power for a gate dimension of 1.0μm ×100μm devices. The DCFETs performs a higher gate leakage current than that in A-DCFETs versus input power levels, and both leakage currents increase by increasing the input RF powers. The linear power gain is 16.2 dB for A-DCFETs and is 15.5 dB for DCFETs. The maximum output power is 13.8 dBm for A-DCFETs and is 11.3 dBm for DCFETs. The power-added efficiency (PAE) curves versus the input power under 2.4GHz are shown in Fig. 5(b). The maximum PAE is 45.4 % for A-DCFETs and is 40 % for DCFETs at an input power of 5 dBm and 3 dBm, respectively. As shown in Fig. 5(a), the microwave power performance is improved by the air-bridge gate process, and the power gain degradation is also suppressed in the high input power regime.

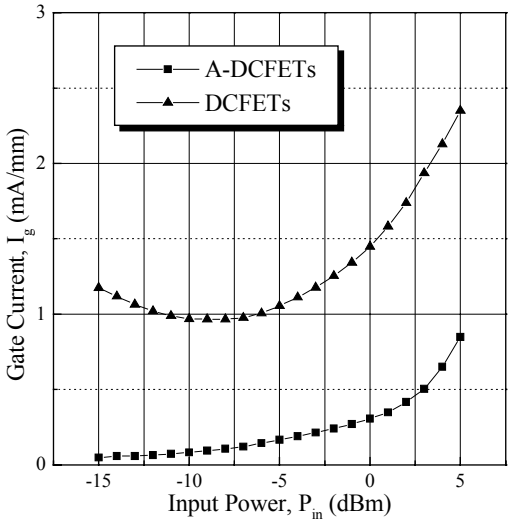
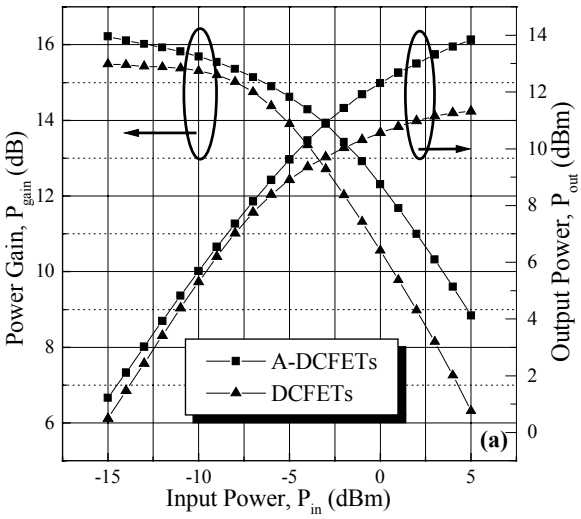



Fig. 5 Gate leakage current versus input power of A-DCFET and DCFETs for 1μm x 100μm device



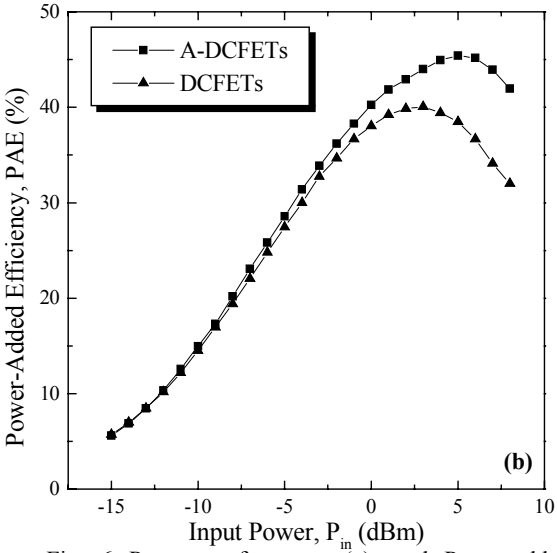



Fig. 6 Power performance (a), and Power-added efficiency (b) of A-DCFETs and DCFETs with a gate length of 1μm at 2.4 GHz.

The reduction of gate leakage and parasitic capacitances in A-DCFETs provides a significant improvement in device linearity. The third-order inter-modulation of the device versus the input power, an important index of device linearity, was carried out by injecting two-tone frequencies, i.e. 2.400 GHz and 2.401 GHz. Fig. 7 shows the measured IM3 and the fundamental output power as a function of the input power for both devices. The third-order intercept point ($OIP_3$) at output is 16.8 dBm in A-DCFETs, and this value is 14.8 dBm in DCFETs. In addition, as to the power ratio between the fundamental frequency and IM3 products, A-DCFETs demonstrates a much better performance than that of the conventional DCFETs, i.e. 22.8 dBc for A-DCFETs and 15.8 dBc for DCFETs at a input power of 0 dBm.

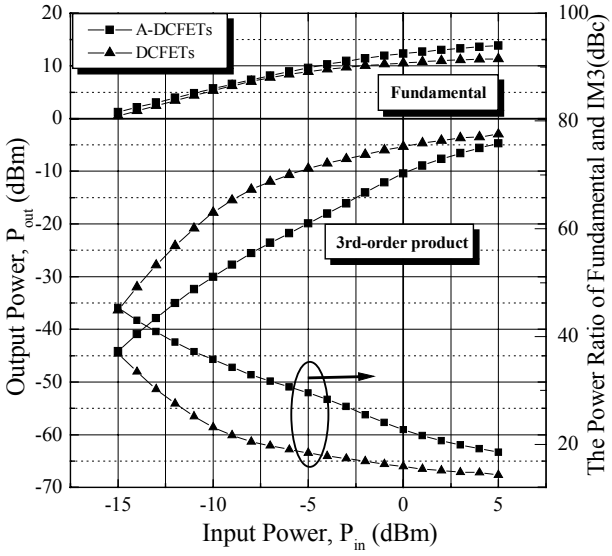



Fig. 7 The Output power performance and third order intermodultion products for both devices.

## IV. CONCLUSION

We proposed a novel fabrication process technique for improving the linearity of AlGaAs/InGaAs power doped-channel FETs. By using this air-bridge gate technique, we demonstrate that the reduction of gate leakage and parasitic capacitance is an effective way to improve the device power performance and reduce the IM3 products under high input power levels. Therefore, A-DCFETs illustrate great power performance for applying in wireless communication system.

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